Performance Modeling of a Network Processor Data Path Using Queuing Systems

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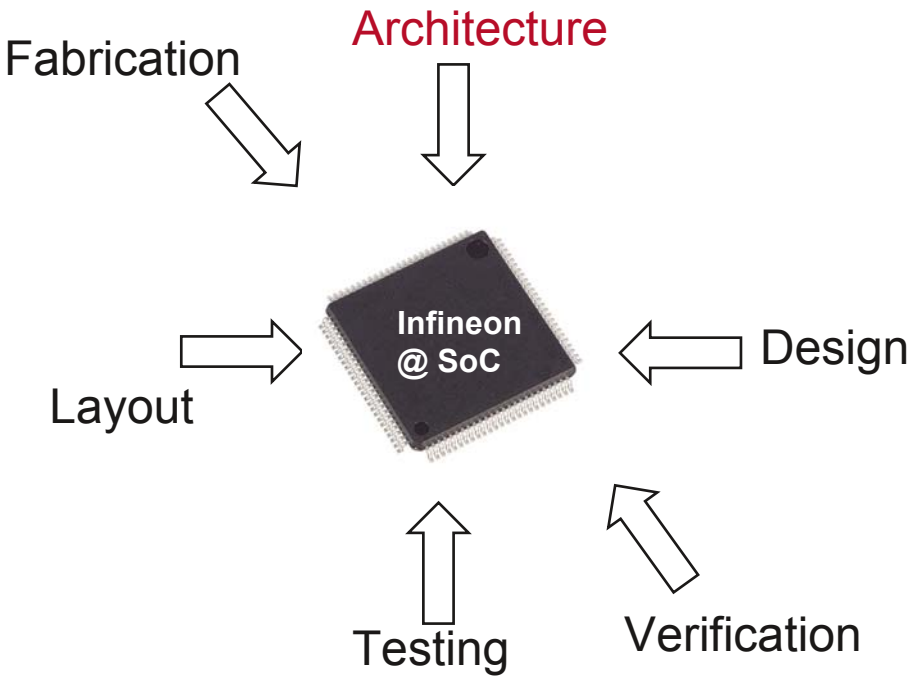
Never stop thinking

Outline

1. **Motivation**
2. **Introduction to SystemQ**
3. **Case Study**
4. **Analysis of Case Study Results**

Phases of SOC development



Our focus –

Performance Modeling of Network Processor Datapath during Architecture Phase.

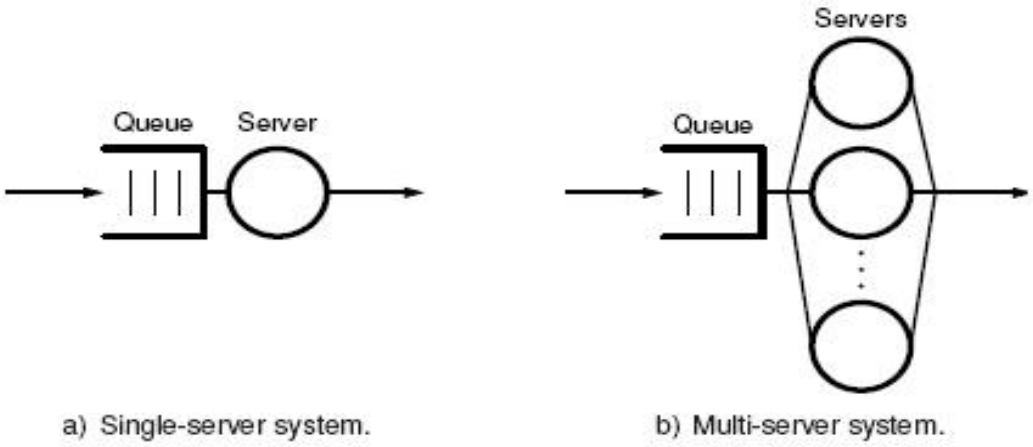
Need for Performance Evaluation

- Architectural phase
  - Identification of hardware resources (memories, logic gates etc)
  - Selection of scheduling algorithms
  - Mapping of functionality to computing models

  - Performance Evaluation during Architecture phase results in

    - Right architecture
    - Optimal chip area
    - Reduced latencies
    - Optimal memory size
    - Optimal power consumption.

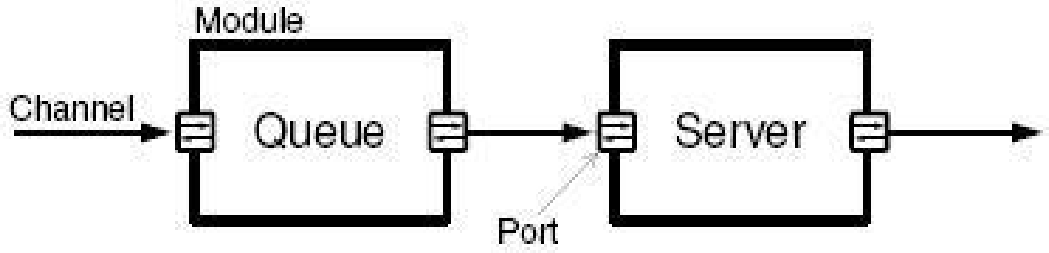
Overview of Queuing Systems



a) Single-server system. b) Multi-server system.

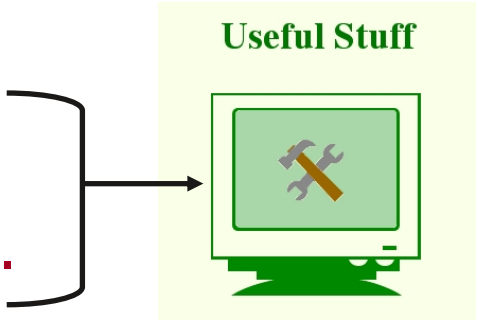
- Queue – Waiting rooms for the request
  - Serves transactions to Server based on SIRO,FCFS etc.
  - Does not modify/alter the contents of the transaction
  - Equivalent of buffer (memory) in Hardware implementation
- Server – Process the transaction by taking finite time
  - Service time ($T_{service}$) – Constant or varying based on request type.

SystemQ based Simulation platform

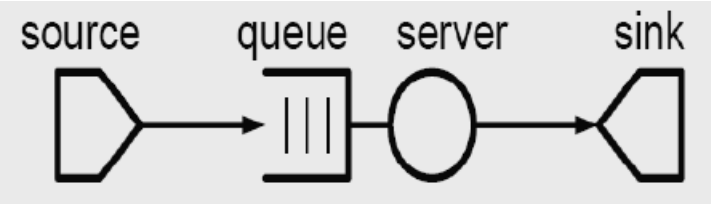


- Based on Queuing Systems
- Built using SystemC communication method
- Performance level of abstraction
- Supports parameterized re-configuration for simulation runs
- Functional, Structural and Communication refinement possible

- Information from Analysis
  - Queue lengths
  - Server Utilization
  - Residence transaction times.



SystemQ based Simulation platform(Contd)



- Source
  - Generates transactions based on "time" - "length" distribution
  - Encapsulation based on desired protocol stack
    - Protocol stack examples – Ethernet, ATM etc..
- Sink
  - Packet arrival rates (throughput measurement).

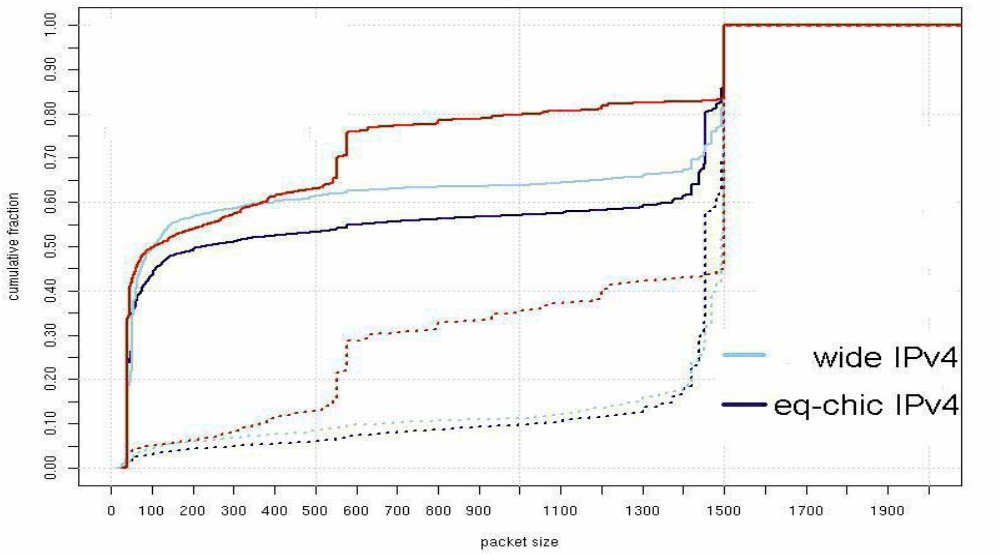
Choosing appropriate Stimuli

- Conventional packet length distribution
  - IMIX
    - Widely adopted packet distribution
    - Distribution of 64:594:1518 byte packets in ratio of 7:4:1
    - In percentages 58%:33.3%:8.3%

- Packet length distribution used in our approach
  - Real time internet traces published by CAIDA
  - Arrived at more realistic internet packet distribution.

Choosing appropriate Stimuli (Contd 1)

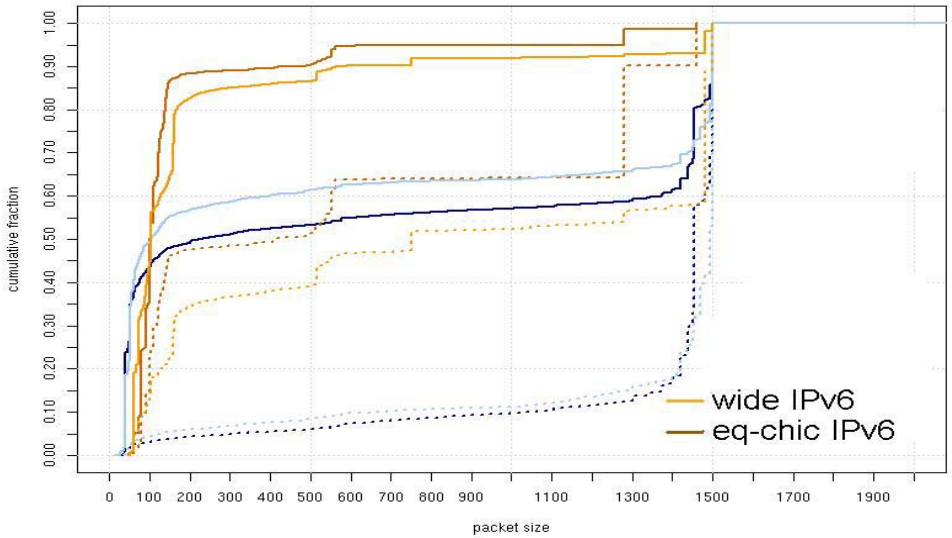
Cumulative IPv4 packet size distribution in 2008



US: "Eq-Chic"	No of Packets in G	Percentage of IPv4 packets
64 - 146	0.8225	47%
147 - 530	0.1225	7%
531 - 1426	0.1225	7%
1427 - 1518	0.6825	39%
Japan: "WIDE"		
64 - 146	2.1774	57%
147 - 530	0.191	5%
530 - 1426	0.2674	7%
1427 - 1518	1.1842	31%

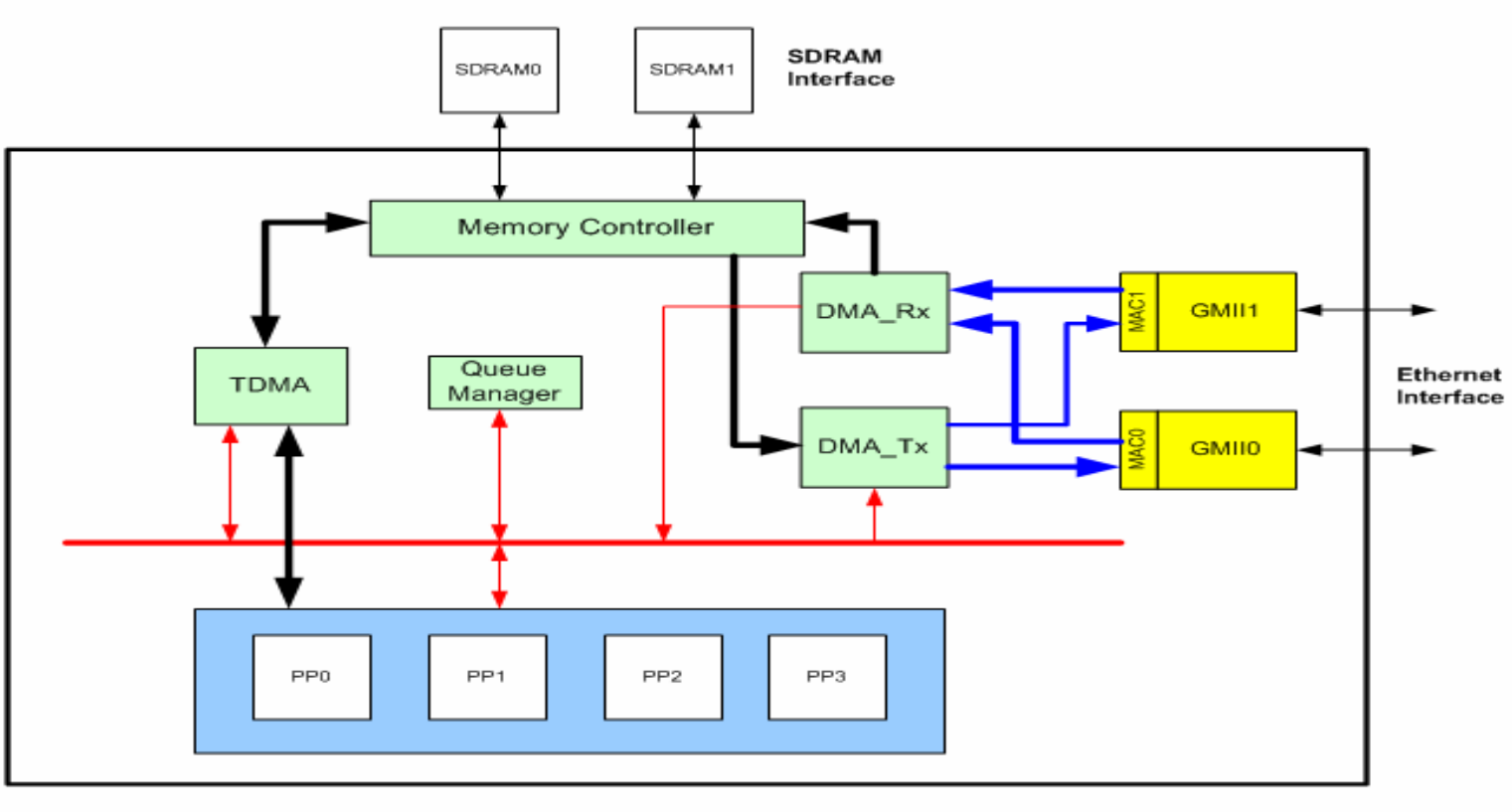
Choosing appropriate Stimuli (Contd 2)

Cumulative IPv4 and IPv6 packet size distribution in 2008

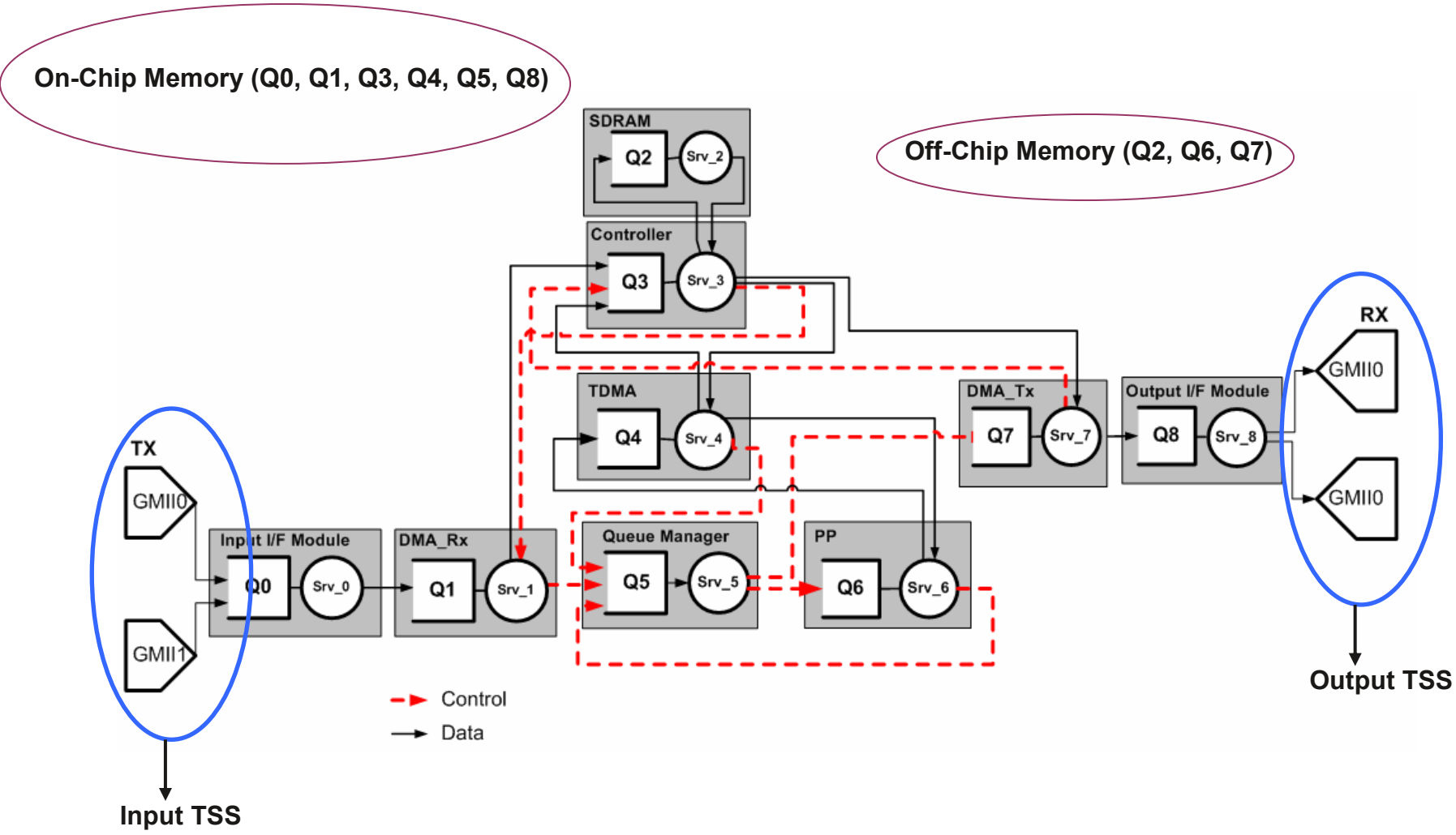


US: "Eq-Chic"	No of Packets in K	Percentage of IPv6 packets
64 - 146	41.8	55%
147 - 274	25.08	33%
275 - 658	4.56	6%
659 - 1298	1.52	2%
1299 - 1518	3.04	4%
Japan: "WIDE"	**No of Packets in M**	
64 - 146	6.05	55%
147 - 274	3.08	28%
275 - 658	0.66	6%
659 - 1298	0.33	3%
1299 - 1518	0.88	8%

Typical Network Processor Datapath



Representation of NWP in SystemQ



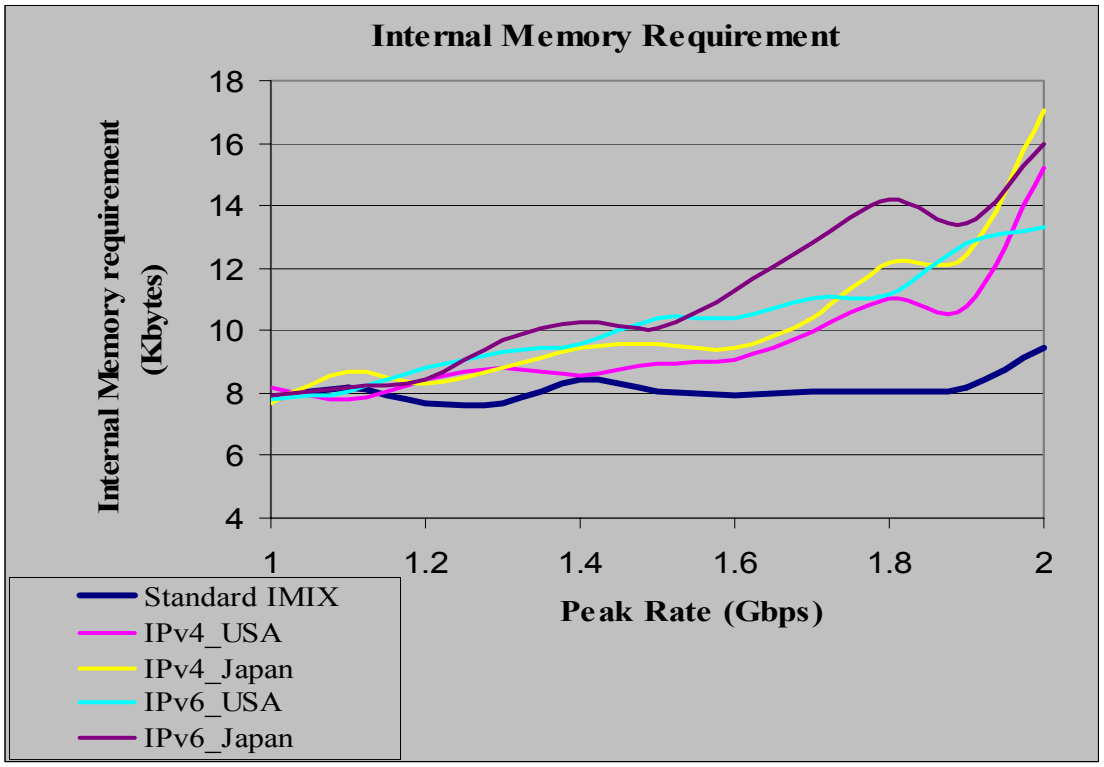
Simulation Setup

- Service times of each servers (packet latency)
  - Specified by the individual modules
- Two TSS (Transfer Source/Sink) for 2 Gigabit Ethernet ports
- Internal segment size of packet based on the architecture
- Total simulation time – 500milliseconds
- Rates, service times of modules etc., are specified in a parameter file.

Simulation Parameters

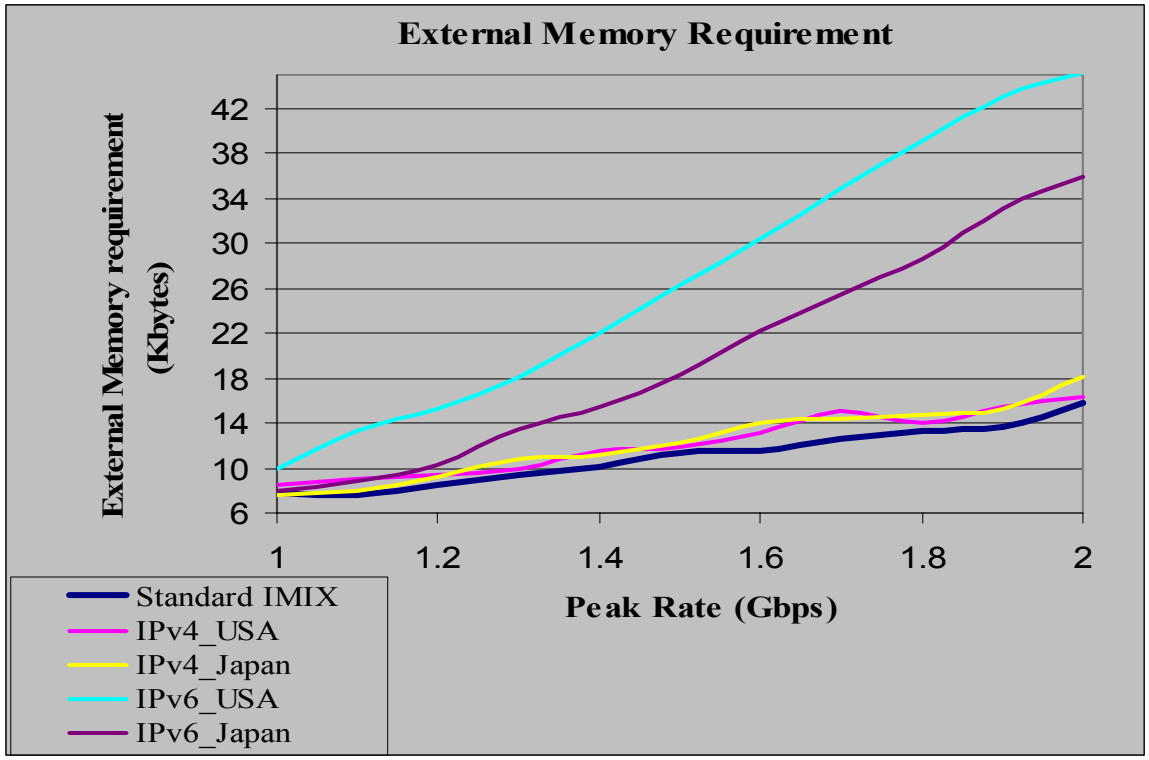
- Stimuli
  - Standard IMIX
  - IPv4 packets from US and Japan traces (CAIDA)
  - IPv6 packets from US and Japan traces (CAIDA)
- TSS
  - Sustainable rate – 1Gbps
  - Peak rates varied from 1Gbps-2Gbps
- $T_{service}$ for Protocol processor – 1000 cycles/packet
- $T_{service}$ for DMA_Rx – 64 cycles
- Queue Sizes – Kept as infinite to avoid packet discards.

Simulation Results ~ On-Chip Memory Requirements



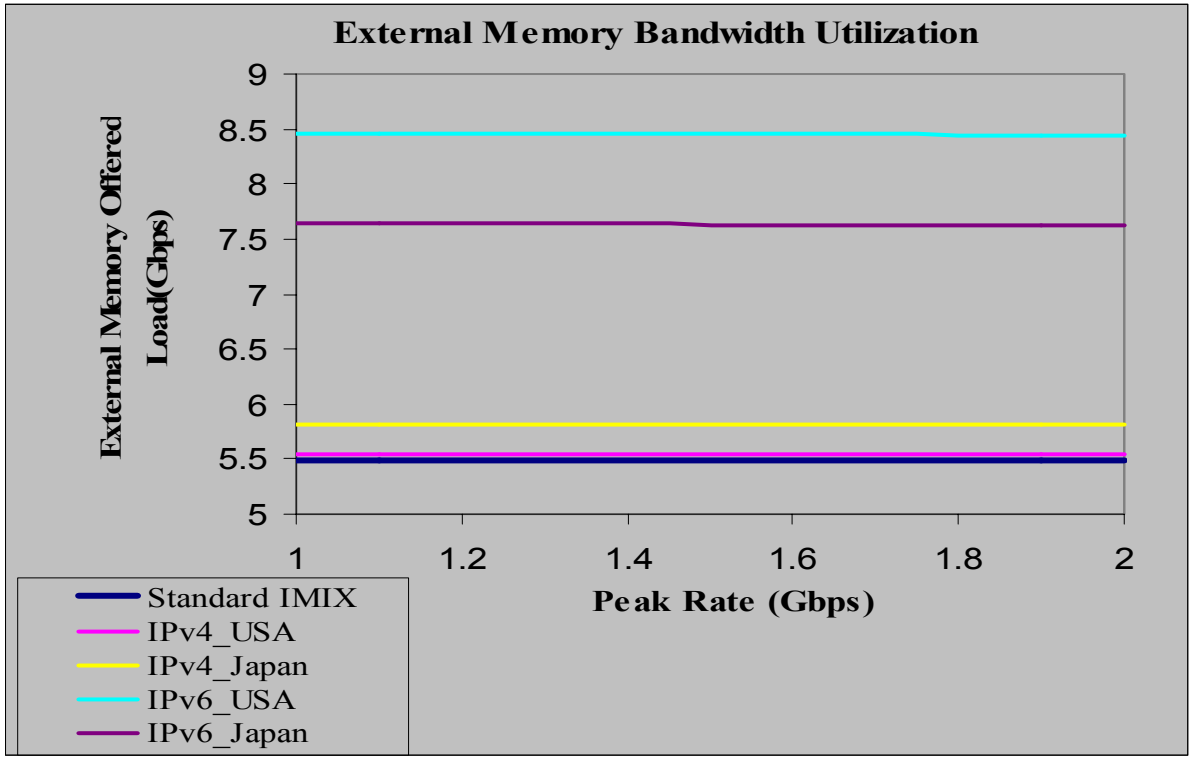
- Standard IMIX plot is below IPv4 and IPv6 plots
- At 2Gbps Peak Rate difference between IMIX and
  - IPv4_Japan and IPv4_USA difference is 8KB and 6KB
  - IPv6_Japan and IPv6_USA difference is 7KB and 4KB.

Simulation Results ~ Off-Chip Memory Requirements



- Standard IMIX plot is below other IPv4 and IPv6 plots
- IPv4 plots almost follows IMIX plot
- At 2Gbps Peak Rate difference between IMIX and
  - IPv6_Japan and IPv6_USA difference is 20KB and 30KB.

Simulation Results – Off-chip memory Bandwidth Utilization



- Offered load varies for different packet length distribution
- No variation of Offered load of SDRAM Vs Peak Rate
- Reason is, 2 banks of SDRAMS are used, which suffice the B/W requirement.

Conclusion

- A basic Network Processor chip model developed, and presented a methodology to evaluate the performance of the Network Processor Data Path
- Stimuli generation is based on Real time internet traffic patterns across different geographical region
- Benefits of this methodology
  - Saving of chip area
  - Saving of cost
  - Throughput requirements are met
- This methodology can be applied to any SOC development during the architectural phase to arrive at refined and optimized architecture.

Thank You